IN THE SPECIFICATION

Please insert the following paragraphs starting at line 6 of Page 16 with the following paragraph:

In one embodiment, system management controller 130 comprises control logic to allocate executable transactions within the multicore processor to one of the processor elements in accordance with one of a range of pre-defined allocation parameters. The control logic is in communication with each of the plurality of interconnected processor elements via a plurality of controller clients. Each of the controller clients is associated with a corresponding interconnected processor element and each controller client is configured to control communication between each associated interconnected processing element and the rest of the multicore processor. The control logic may be separate from a master processing element.

Each executable transaction to be allocated can include threads, each of which form part of an application being executed upon the multicore processor. In one embodiment, at least some of the threads are independent threads capable of execution independently of other events, and at least some of the threads are dependent threads, whose execution is dependent upon the existence of a predetermined event.

In one embodiment, the control logic further comprises an executable transaction manager and a dedicated memory manager. The dedicated memory manager controls access by the executable transaction manager to a dedicated memory. The executable transaction manager can further comprise an executable

transaction input manager, configured to maintain an indication of available memory within the dedicated memory. The executable transaction input manager can be configured to maintain a list of available memory locations within the dedicated memory. The executable transaction input manager can maintain the indication of available memory as a result of updated instructions from the dedicated memory manager. The control logic can further comprise a time manager configured to provide timer functions to the executable transaction manager.

In another embodiment, the executable transaction manager further comprises an executable transaction synchronisation manager, configured to maintain at least one pending queue list within the dedicated memory, indicative of dependent threads awaiting the occurrence of a predetermined event, and at least one timer queue list within the dedicated memory, indicative of threads awaiting a timing event.

In one embodiment, the executable transaction manager further comprises an executable transaction output manager configured to maintain a plurality of dispatch queue structures within the dedicated memory, indicative of the threads awaiting execution on an associated one of the processor elements, and to maintain a plurality of ready queue structures within the dedicated memory, indicative of threads awaiting allocation to a one of the processor elements for execution there.

In another embodiment, the executable transaction manager further comprises an executable transaction schedule manager, configured to provide and maintain

scheduling decisions for prioritising the dispatch of threads from within the ready queues to the dispatch queue for each processor element.

In one embodiment, the control logic further comprises a system interface manager, in communication with the executable transaction manager, and configured to manage access by the controller to the multicore processor. The system interface manager can be arranged to provide interconnect interfacing and configuration and run-time access to the executable transaction manager.

In another embodiment, the control logic further comprises a system interrupt manager, for converting system interrupts in a first format employed within the multicore processor, into controller interrupts in a second, different format, which second format is understandable by the executable transaction manager.